

JAWAHARLAL NEHRUTECHNOLOGICALUNIVERSITY: KAKINADA

KAKINADA-533003, Andhra Pradesh, India

R-13 Syllabus for IT.JNTUK

II Year-I Semester		T	P	C
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	Digital Logic Design (RT21053)			

Course Description and Objectives:

- To introduce the basic tools for design with combinational and sequential digital logic and state machines.
- To learn simple digital circuits in preparation for computer engineering.

Course Outcomes:

Upon completion of the course, the student will be able to achieve the following outcomes.

Cos	Cours eOutcomes	POs
1	Define different number systems, binary addition and subtraction, 2's complement representation and apply operations with this representation.	
2	Define various logic gates, discuss about Boolean algebra and apply minimization using K-Maps.	
3	Discuss various combinational logic circuits.	3
4	Discuss various sequential logic circuits.	5
5	Describe about registers and counters.	2
6.	State different programmable logic devices and compare them.	5

Syllabus:

UNIT I:

Number Systems

Binary, Octal, Decimal, Hexadecimal Number Systems. Conversion of Numbers From One Radix To Another Radix,r's Complement and (r-1)'s Complement Subtraction of Unsigned Numbers, Problems, Signed Binary Numbers, Weighted and Non weighted codes

UNIT II:

Logic Gates And Boolean Algebra: Basic Gates NOT, AND, OR, Boolean Theorms, Complement And Dual of Logical Expressions, Universal Gates, Ex-Or and Ex-Nor Gates, SOP, POS, Minimizations of Logic Functions Using Boolean Theorems, Two level Realization of Logic Functions Using Universal Gates. Gate Level Minimization: Karnaugh Map Method (K-Map): Minimization of Boolean Functions maximum upto Four Variables, POS and SOP, Simplifications With Don't Care Conditions Using K-Map.

UNIT III:

Combinational Logic Circuits

Design of Half Adder, Full Adder, Half Subtractor, Full Subtractor, Ripple Adders and Subtractors, Ripple Adder/Subtractor Using Ones and Twos Complement Method.

Design of Decoders, Encoders, Multiplexers, Demultiplexers, Higher Order emultiplexers and Multiplexers, Priority Encoder, Code Converters, Magnitude Comparator.

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UNIT IV:

Introduction to Sequential Logic Circuits: Classification of Sequential Circuits, Basic Sequential Logic Circuits: Latch and Flip-Flop, RS- Latch Using NAND and NOR Gates, Truth Tables. RS,JK,T and D Flip Flops , Truth and Excitation Tables, Conversion of Flip Flops. Flip Flops With Asynchronous Inputs (Preset and Clear).

UNIT V:

Registers and Counters: Design of Registers, Buffer Register, Control Buffer Registers, Bidirectional Shift Registers, Universal Shift Register, Design of Ripple Counters, Synchronous Counters and Variable Modulus Counters, Ring Counter, Johnson Counter.

UNIT VI:

Introduction to Programmable Logic Devices (PLDs):PLA, PAL, PROM. Realization of Switching Functions Using PROM, PAL and PLA. Comparison of PLA, PAL and PROM.

TEXT BOOKS:

- 1. Digital Design ,4/e, M.Morris Mano, Michael D Ciletti,PEA
- 2. Fundamentals of Logic Design, 5/e, Roth, Cengage

REFERENCE BOOKS:

- 1. Switching and Finite Automata Theory, 3/e, Kohavi, Jha, Cambridge.
- 2. Digital Logic Design, Leach, Malvino, Saha, TMH
- 3. Modern Digital Electronics, R.P. Jain, TMH